This Page Is Inserted by IFW Operations and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents will not correct images, please do not report the images to the Image Problem Mailbox.

SOURCE CODE APPENDIX

```
Software UART for SPI-to-RS232 for National Semiconductor's COP8SAx
                            Rev 0.1, February 20, 1998
        > Configured for COP8SAC @ 10MHz
        > Hardware target = COP8-EVAL-HI01 (COP8 Evaluation Board)
        > Uses "HyperTerminal" under Windows 95
                           . by: Steven Goldman
                                   National Semiconductor
                                   Senior Field Applications Engineer
        .TITLE SPI-232
        .CHIP 8SAC
.SECT MAIN,ROM,ABS=0
; DECLARATIONS:
                                   ; PORTF Data Reg
; PORTF Config Reg
; PORTF Register (Input Only)
           PORTFD
                   = 0 \times 94
           PORTFC
                   = 0x95
           PORTFP = 0 \times 96
                                   ; Dip Switches ; LED's
           DIPS
                    = 0x96
           LEDS
                    = 0 \times DC
           TAURLOB = 0E6
                                    ; Timer B Reload, Low
           TAURHIB = 0E7
                                    ; Timer B Reload, High
           TIMERLO = OEA
           TIMERHI = 0EB
           TAURLO = 0EC
                                    ; Timer A Reload, Low
           TAURHI = 0ED
                                    ; Timer A Reload, High
           CNTRL
                    = OEE
           PSW
                    = OEF
           PORTLD
                   = 0D0
           PORTLC
                   = 0D1
           PORTLP
                    = 0D2
           PORTGD
                   = 0D4
           PORTGC
                    = 0D5
           PORTGP
                    = 0D6
           R0
                    = 0F0
                    = 0F1
           R1
           TRUN
                    = 4
           TPND
                    = 5
           RECREG
                    = 020
                                   ; REG TO HOLD RECEIVED DATA.
           STKPTR
                    = 0 \times FD
                                     ; Stack Pointer
```

```
; RECEIVE PORTION
      1/9600 BAUD = 104 uSEC/BIT DECIMAL = 0068 HEX
      1/2 BIT TIME IS = 52 uSEC = 52 DECIMAL = 0034 HEX.
                                      ; Setup PortF as INPUT
            LD PORTFC, #0x00
START:
            LD A, DIPS
IFEQ A, #0x00
                                      ; Dislay Revision Number
            JMP REVNUM
            IFEQ A, #0x01
JMP RECROUT
                                       ; Receive Routine
            IFEQ A, #0x02
                                       ; Transmit Routine
            JMP CALLXMIT
            IFEQ A, #0x03
JMP DEBUG1
                                       ; Toggles RXD line
                                       ; Transmit "N"
            IFEQ A, #0x04
            JMP SEND N
            LD A, #0xFF
JSR ATOLEDS
                                        ; Error Trap
             JMP HERE
            LD A, #0x17
JSR ATOLEDS
JMP HERE
REVNUM:
                                    ; Displays the Routine Number (3)
; Make sure it is input pin
; Configure RXD pin as OUTPUT
DEBUG1:
             JSR ATOLEDS
            RBIT 0, PORTLC
SBIT 1, PORTLC
LD B, #PORTLD
SBIT 1, [B]
RBIT 1, [B]
 TOGGLE:
             JP TOGGLE
 RECROUT: JSR ATOLEDS
             RBIT 0, PSW
LD SP, #02F
                                   ; Disable all interrupts.
                RC
             LD PORTGC ,#0x08 ; SET UP G1,& G2 AS INPUTS.
LD PORTLC, #0x0E ; Set up L0 as input, L1/L3
SBIT 1, PORTLD
RBIT 3, PORTLD
                                        ; Set up LO as input, L1/L3 as output.
```

```
;
STRTRX:
              CLRA
              RBIT 3, PORTLD
RBIT TRUN, CNTRL
LD TIMERLO, #0x0E
LD TIMERHI, #0x00
LD TAURLO, #0x62
                                                ; Make sure timer1 is off.
                                               ; Load Half timer LB
; Load Half timer HB
                                               ; Load Baudrate LB
SETIMR:
              LD TAURHI, #0x00
LD TAURLOB, #0x00
LD TAURHIB, #0x00
LD CNTRL, #0xA0
                                                ; Load Baudrate HB
                                                 ; (n-1) Data bits=8
                LD R1, #0x08
IDLE:
              IFBIT 0, PORTLP
                JP TRIGGER
JP IDLE
                RBIT 2, PORTLD
TRIGGER:
              SBIT 3, PORTLD
              SBIT TRUN , CNTRL RBIT TPND , PSW IFBIT TPND , PSW
                                              ; Start Timer
; Reset Interrupt pending flag
CHECK:
                                              ; Test Int flag
CHECK0:
              JP CONTST
JP CHECKO
                              CNTRL
                                              ; Stop the timer
               RBIT TRUN,
CONTST:
               SBIT TRUN, CNTRL
RBIT TPND , PSW
IFBIT 0, PORTLP
                                                ; Start the timer
                                               ; Reset Interrupt Pending flag
                                                ; Test for valid Start Bit
                 JP VALSTART
                 JP STRTRX
VALSTART: SBIT 2, PORTLD RBIT 2, PORTLD
RECEV:
               IFBIT TPND, PSW
                                               ; Receive bit in the middle
CHECK1:
               JP CONT
JP CHECK1
RBIT TRUN, CNTRL
CONT:
                                               ; Stop the timer
                 SBIT TRUN, CNTRL
RBIT TPND, PSW
                                                 ; Start the timer
               SBIT 2, PORTLD
RBIT 2, PORTLD
                                                ; Sampling pulse, per bit
                                                ; Load receive buffer
               LD A, RECREG
                                               ; Assume this was at Ground, then "1"; If at +5VDC, then "0"; Reset Carry is skipped if "1"; Either way, rotate Right
               SC
               IFBIT 0, PORTLP
               RC
               RRCA
               X A, RECREG
DRSZ R1
                                                ; Store as latest value
                                                ; Are we done yet?
```

; No...get more

JP RECEV

```
FINISH:
          SBIT 3, PORTLD
                                 ; Golly! We are almost done
          LD A, RECREG
                                 ; Display byte
          JSR ATOLEDS
          RBIT 3, PORTLD
                                 ; Trigger scope (end of frame)
          JP STRTRX
                                 ; Go get more
                   ; Value must be in Accumulator
ATOLEDS:
                               Since 1=LED Off, "A" must
become NOT A (or /A). Inverted
                           ;
                               value is then displayed. Flow
                               returns to caller.
         IFEQ A, #0X0D
                               ; If carriage return (0x0D), return.
         RET
         XOR A, #0xFF
                                ; Invert each bit
        LD B, #LEDS
X A, [B]
LD A, LEDS
                                ; Transfer /A to LED's
         XOR A, #0xFF
         RET
HERE:
          JMP HERE
                                 ; Subroutine used to wait
                                    ; for Reset
TRANSMISSION PORTION
      Generic Calling Routine
XMIT:
                                 ; Soft UART Transmit routine
                                     Uses L.1 as an output
                                     Assumes L.O is input
                                     Supports Half-duplex mode
          SBIT 3, PORTLC
SBIT 1, PORTLC
RBIT 0, PORTLC
                                 ; Set TRIGGER (L.3) as output
; RXD (send to PC)
; TXD (from PC)
          LD TIMERLO, #0x62
LD TIMERHI, #0x00
LD TAURLO, #0x62
LD TAURHI, #0x00
                                 ; Setup Timers
          LD TAURLOB, #0x00
LD TAURHIB, #0x00
          LD CNTRL, #0xA0
          LD R1, #0x08
                                 ; Set for 8 data bits
          RBIT 3, PORTLD
                                 ; Set TRIGGER (L.3) LOW for frame sync
```

```
; Set TRIGGER (L.3) HIGH for frame sync ; Transmit Start Bit (0)
           SBIT 3, PORTLD RBIT 1, PORTLD
           JSR WFOBT
                                     ; Wait For One Bit Time
                                     ; More next bit to "CARRY"
MOREBITS: RRCA
                                     ; Assume we XMIT "0"
           RBIT 1, PORTLD
           IFC
                                     ; Are we wrong?
           SBIT 1, PORTLD
                                    ; Sorry, XMIT "1"
; Either way, wait
           JSR WFOBT
           DRSZ R1
           JMP MOREBITS
SENDSTOP: SBIT 1, PORTLD
           JSR WFOBT
                                     ; Return to calling routine
           RET
           SBIT TRUN, CNTRL
IFBIT TPND, PSW
JP BT_DONE
WFOBT:
                                     ; Wait For One Bit Time
                                     ; Get ready for next one
           JP WFOBT
BT_DONE: RBIT TPND, PSW
                                   ; Reset Timer
                                     ; Return to Calling Routine
           RET
CALLXMIT: LD LEDS, #0xF8
LD A, #'C'
                                     ; Transmit "COP8-"
            JSR XMIT
           LD A, #'0'
           JSR XMIT
            LD A, #'P'
            JSR XMIT
            LD A, #'8'
            JSR XMIT
            LD A, #'-'
            JSR XMIT
            JMP CALLXMIT
                                     ; Do it again, & again, & again...
           LD LEDS, #0xFB
LD A, #'N'
SEND N:
AA:
           JSR XMIT
JMP AA
```

.END START